SEMICONDUCTOR DEVICE INCLUDING A MULTI-CHANNEL FIN FIELD EFFECT TRANSISTOR INCLUDING PROTRUDING ACTIVE PORTIONS AND METHOD OF FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device including a multi-channel fin field effect transistor (FinFET) and a method of fabricating the same. More particularly, the present invention relates to a semiconductor device including a multi-channel FinFET in a cell and/or peripheral circuit region of a semiconductor substrate and a method of fabricating the same.

2. Description of the Related Art

In order to improve performance and reduce fabrication cost of semiconductor devices, an integration density of semiconductor devices must continually increase. Increasing integration density of semiconductor devices requires developing techniques for reducing a feature size of a semiconductor device.

In conventional semiconductor fabricating processes, the channel length of a metal-oxide-semiconductor field effect transistor (MOSFET) is decreased to increase an operating speed and integration density of a semiconductor device. This decrease in channel length, however, may degrade characteristics of the device as an active switch. For example, as a distance between a source and a drain is further reduced, a short channel effect occurs. Thus, it becomes difficult to effectively suppress an influence of a drain electrical potential on a source electrical potential and a channel electrical potential. However, since a conventional MOSFET, in which a channel is disposed parallel on a surface of a semiconductor, is a planar channel device, it is difficult to not only structurally scale down the MOSFET, but also to suppress the occurrence of the short channel effect.

A FinFET has a structure, in which a fin-shaped, three-dimensional active region is formed, and both lateral surfaces and a top surface of the fin-shaped active region are surrounded by a gate. Thus, the FinFET includes not a planar channel but a three-dimensional channel. Unlike a planar MOSFET, since the FinFET includes a vertical channel disposed on a substrate, the size of the FinFET can be scaled down, and a short channel effect may decrease by greatly reducing a junction capacitance of a drain. In addition, the FinFET offers other superior electrical properties such as higher drive current and lower leakage current induced by improved sub-threshold current and reduced drain induced barrier lowering (DIBL). Accordingly, in view of these advantages of the FinFET, extensive research into replacing conventional MOSFETs with FinFETs has recently been conducted.

Although the FinFET offers these superior electrical characteristics, it is currently difficult to make a FinFET having a very short and uniform channel width transistor, e.g., less than 30 nm, because of the limitations of current lithography techniques. These limitations lead to other disadvantages. For example, if fins are not formed to a uniform width, a current dispersion characteristic may be deteriorated. To form a three-dimensional channel on a substrate in a FinFET, a photolithography process must be performed. However, a line width that can be obtained by the photolithography process is limited. Therefore, an improved method for forming a three-dimensional channel having a fine line width below a resolution limit is required.

Moreover, to appropriately control a current increased by forming a FinFET in a cell region, a transistor of a peripheral circuit region requires change. However, the layout of a conventional active region should be adjusted in accordance with a new fin structure to form a FinFET in a peripheral circuit region, and photoresist trimming should be used to obtain a fine line width. Thus, it is difficult to increase a contact region of a source and a drain due to the above-described patterning problems.

By fabricating a relatively short multi-channel transistor of a fin type, the transistor's drive current level may be increased. Therefore, new semiconductor devices including multi-channel FinFETs having uniform and relatively short channel width and methods of fabricating the same are needed.

SUMMARY OF THE INVENTION

The present invention is therefore directed to a semiconductor device including a multi-channel FinFET and a method of fabricating the same, which substantially overcome one or more of the problems due to the limitations and disadvantages of the related art.

It is a feature of an embodiment of the present invention to provide a semiconductor device including a multi-channel FinFET and a method of fabricating the same, wherein the multi-channel FinFET has a uniform fine line width disposed in either a cell region and/or a peripheral circuit region.

It is another feature of an embodiment of the present invention to provide a semiconductor device including a multi-channel FinFET and a method of fabricating the same, wherein the multi-channel FinFET has a short and uniform channel width.

It is yet another feature of an embodiment of the present invention to provide a semiconductor device including a multi-channel FinFET and a method of fabricating the same that significantly increases an effective channel length of the transistor.

It is still another feature of an embodiment of the present invention to provide a semiconductor device including a multi-channel FinFET and a method of fabricating the same that is able to increase a current level of a transistor, thereby increasing an operating speed of the semiconductor device, by providing a plurality of fin-type active channels in the transistor.

It is yet still another feature of an embodiment of the present invention to provide a semiconductor device including a multi-channel FinFET and a method of fabricating the same that is able to produce a lower cost FinFET gate having a plurality of fin-type active channels using a simplified manufacturing process.

It is a further feature of an embodiment of the present invention to form a transistor having one or more three-dimensional channels in a single active region by forming fins having a uniform fine line width in a cell region and/or a peripheral circuit region of the semiconductor device.

At least one of the above features and other advantages may be provided by a semiconductor device including a semiconductor substrate having a cell region and a peripheral circuit region, a portion of the semiconductor substrate in the cell region and in the peripheral circuit region including an isolation region defining an active region, a portion of the active region protruding above an upper surface of the isolation region to define at least two active channels, a gate dielectric layer formed over the active region of the semiconductor substrate including the at least two protruding active channels, a gate electrode formed over the gate dielectric layer and